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In this quarter, we conducted a performance evaluation of the proposed optical architecture SPARO (Symbolic Processing Architecture in Optics). Specifically, we examined the performance of the ring interconnection network of SPARO. An accurate performance model was developed for predicting the message throughout of bidirectional ring network. As suspected earlier, the ring network was the bottleneck in the performance. This led us to study other network topologies that are both feasible in optics and yield high throughput. The final choice of the optical interconnection network topology was deemed by the replicated perfect shuffle network.

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OPTICAL SYMBOLIC PROCESSOR FOR EXPERT SYSTEM EXECUTION

Quarterly R&D Status Report No. 5

For the period from 1 June 1987 to 31 August 1987

ARPA Order No. 5794
Program Code 6D10
Period of Performance: 1 June 1987 to 30 May 1987
Amount of Contract: $508,044
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Air Force Office of Scientific Research

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Approved by: D Fulkerson Date: 9/9/87
D. Fulkerson
Department Manager

87 11 3 382

INTRODUCTION

The goal of this program is to develop a concept for an optical computer architecture for symbolic computing by defining a computation model of a high level language, examining the possible devices for the ultimate construction of a processor, and by defining required optical operations.

PROGRESS FOR THE PERIOD

In this quarter we conducted a performance evaluation of the proposed optical architecture SPARO (Symbolic Processing Architecture in Optics). Specifically, we examined the performance of the ring interconnection network of SPARO. An accurate performance model was developed for predicting the message throughput of bidirectional ring network. As suspected earlier, the ring network was the bottleneck in the performance. This led us to study other network topologies that are both feasible in optics and yield high throughput. The final choice of the optical interconnection network topology was deemed to be the replicated perfect shuffle network.

The following are the major accomplishments for this quarter:

Performance evaluation of the ring interconnection network

We derived an accurate analytical model of unidirectional and bidirectional ring interconnection networks for predicting the message throughput. The results obtained from the analytical model were later verified by simulation. Both sets of results showed remarkably close agreement. When messages exhibit no locality, the throughput for a 1K processor network is limited to 8. With local messages, the maximum throughput for the same network is 27.

Selection of alternate interconnection network topology

The analysis of the ring network revealed that although a register-based ring network may be easy to construct, its performance for highly parallel computing is unacceptable, especially when the number of processors are more than 100. Since we are proposing fine-grained processing in optics, the number of processors to be considered is 1K or more. The discovery of poor performance by large rings motivated us to examine alternate high-performance interconnection network topologies that can be implemented in optics. Among the possible alternatives, we examined directly connected networks such as hybercubes, multi-stage (indirect-connected) interconnection networks (MINs) such as delta networks, and the replicated single-stage shuffle-exchange network (SEN) where a number of parallel SENs are used to interconnect a large number of processors. The replicated SEN appears to be the most promising since it can be implemented in optics and yet not suffer from the blocking problems of the single-stage SEN.

Comparative evaluation of the replicated SEN

The perfect shuffle exchange network appears to be feasible in optics [3]. However, since it was not clear whether its performance was at par with other known networks, we conducted simulations of the different networks under various load conditions. Our results indicate that replicated SENs have performance close to or comparable to other networks such as MINs or hypercubes, and therefore are good candidates for parallel optical and optoelectronic computing.

EXPERIMENTAL OR SPECIAL EQUIPMENT PURCHASED OR CONSTRUCTED

None.

CHANGE IN KEY PERSONNEL

After the departure of Matt Derstine, Aloke Guha, the principal computer architect on the program, has assumed the role of the principal investigator.

INFORMATION DERIVED FROM MEETINGS, VISITS, BRIEFINGS, AND SCIENTIFIC PAPERS

In this quarter we have relied on a number of technical papers for information on the performance of interconnection networks, replicated shuffle-exchange networks, and feasibility of some of these networks in optics. The most relevant papers are listed below.

[1] D.H. Lawrie and D.A. Padua, 'Analysis of message switching with shuffle-exchanges in multiprocessors,' Proc. of the Workshop on Interconnection Networks for Parallel and Distributed Processing, 1980, pp. 116 - 123.

[2] J.H. Patel, 'Performance of processor-memory interconnections for multiprocessors,' IEEE Transactions on Computers, October 1981, pp. 771 - 780.

[3] C.W. Stirk, R.A. Athale, C.B. Friedlander, private communication.

PROBLEMS NEEDING GOVERNMENT ASSISTANCE

None.

DEVIATIONS FROM THE PLANNED EFFORT

Work on the device portion has been postponed until the architecture of the network has been finalized.

UNITED STATES AIR FORCE QUARTERLY CONTRACTOR R & D STATUS REPORT	REPORT FOR QUARTER ENDING. AUGUST 1987
OPTICAL SYMBOLIC PROCESSOR FOR EXPERT SYSTEM EXECUTION	INITIAL CONTRACT PHASE OPTION ONE
TO: U.S.A.F., A.F.S.C. Air Force Office of Scientific Research Building 410 Bolling AFB, DC 20332-6448	FROM: HONEYWELL, INC. PSC 10701 LYNDALE AVE. SO. BLOOMINGTON, MN. 55420

1. Description Of Contract	a. Type : Cost Plus Fixed Fee	b. Contract Number : F49620-86-C-0082
	c. Contract Value : $865,429	

2. EXPENDITURES		3. COMMITMENTS	
a. Costs	b. Fee	a. Materials	b. Subcontracts
$342,461	$0	$0	$116,634

4. Funding Limitation	5. Estimated Date of Completion	6. Estimated Funds to Complete
$523,456	MAY 30, 1988	$865,429